IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicants(s):	Daniel John Devine and David Thompson
Case:	2
Serial No.:	10/787,376
Filing Date:	February 26, 2004
Examiner:	2182
Group:	Jasjit S. Vidwan
Title:	Controller for Peripheral Communications with Processing Capacity for Peripheral Functions

DECLARATION UNDER 37 C.F.R. §1.131

We, the undersigned, hereby declare and state as follows:

1. We are named joint inventors of the invention that is the subject of the above-referenced U.S. patent application. We have assigned our respective interests in the patent application to Agere Systems Inc. ("Agere").

2. The invention was conceived on or before May 13, 2003 and all inventive activity described herein took place in the United States of America.

3. Prior to May 13, 2003, we prepared an Agere System Requirements Document, entitled "USS2827 USB 2.0 Device Controller." A copy of the Requirements Document is attached hereto as Exhibit 1.

4. After preparing the Requirements Document, we prepared an Invention Submission document as required by Agere. On or about July 11, 2003, the Invention Submission document, subsequently assigned Submission No. 124809, entitled "ARM7 Processor based USB 2.0

Device Controller," was submitted to a former Agere in-house patent attorney, Robert P. Marley. The date that the Invention Submission document was Received by Agere IP Law is noted in the upper right hand portion of the document as July 11, 2003. A copy of the Invention Submission document dated July 11, 2003 is attached hereto as Exhibit 2.

5. The Requirements Document and the Invention Submission document describe an invention falling within one or more of the claims of the present application. For example, Applicants note that pending claims 4, 5, 10, 11, 17, and 18 are supported by FIG. 3 and the corresponding discussion of the present application (This figure appears on page 4 of the Requirements Document). Exhibits 1 and 2 provide evidence that the aspects of the invention claimed in claims 4, 5, 10, 11, 17, and 18 and supported by FIG. 3 were conceived on or before May 13, 2003.

6. On or about January 12, 2004, Mr. Kevin Mason and Mr. Daniel Devine, a co-inventor of the above-referenced application, met to discuss the above-referenced application. A copy of an electronic mail message from Mr. Devine to Mr. Mason documenting this meeting is attached hereto as Exhibit 3.

7. On or about February 3, 2004, Mr. Devine provided electronic copies of the disclosure material via electronic mail to Mr. Mason. A copy of an electronic mail message from Mr. Devine to Mr. Mason documenting this exchange is attached hereto as Exhibit 4.

8. On or about February 5, 2004, a first draft of the present application was sent via electronic mail by Mr. Mason to Mr. Devine. A copy of an electronic mail message from Mr. Mason to Mr. Devine documenting this exchange is included in the email history shown in Exhibit 5.

9. On or about February 23, 2004, Mr. Devine approved the draft application. A copy of an electronic mail message from Mr. Devine to Mr. Mason containing this approval is included in the email history shown in Exhibit 5.

10. A final draft was sent via electronic mail to Mr. Devine on February 23, 2004. A copy of an electronic mail message from Mr. Mason to Mr. Devine documenting this exchange is included in the email history shown in Exhibit 6.

11. The final draft was approved by Mr. Devine on February 23, 2004. A copy of an electronic mail message from Mr. Devine to Mr. Mason documenting this approval is included in the email history shown in Exhibit 5.

12. As noted above, the present patent application was filed by Mr. Mason on February 26, 2004.

13. All statements made herein of our own knowledge are true, and all statements made on information and belief are believed to be true.

14. We understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and may jeopardize the validity of the application or any patent issuing thereon.

Date: 10/8/08

Daniel John Devine

Date: _____

David Thompson

9. On or about February 25, 2004, Mr. Devine approved the draft application. A copy of the electronic mail message from Mr. Devine to Mr. Mason containing this approval is included in the email history shown in Exhibit 5.

10. A final draft was sent via electronic mail to Mr. Devine on February 25, 2004. A copy of an electronic mail message from Mr. Mason to Mr. Devine documenting this exchange is included in the email history shown in Exhibit 6.

11. The final draft was approved by Mr. Devine on February 25, 2004. A copy of an electronic mail message from Mr. Devine to Mr. Mason documenting this approval is included in the email history shown in Exhibit 7.

12. As noted above, the present patent application was filed by Mr. Mason on February 26, 2004.

13. All statements made herein of our own knowledge are true, and all statements made on information and belief are believed to be true.

14. We understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and may jeopardize the validity of the application or any patent issuing thereon.

Date: _____

Daniel John Devine

Date: 10/9/06

David Thompson

Exh. 1

May 13, 2003

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USS2827 USB 2.0 Device Controller System Requirements Document

Table of Contents

Introduction

This document defines the requirements of the USS2827 device controller from a system perspective. There is enough detail about the achitecture and interfaces of the device to allow the various development disciplines to begin estimating the effort involved in creating such a device. Some areas will require more detailed specification before actual design begins.

The USS2827 Marketing Requirements Document describes the intended markets for this device and should be used as a reference.

Features

- Integrated ARM7TDMI core operating at up to 120 MHz
- Integrated USB 2.0 device controller.
  - USB revision 2.0 and 1.1 compliant.
  - Self-powered or bus-powered USB device.
  - 2K USB FIFOs.
  - Supports up to 16 USB endpoints.
  - Supports control, interrupt, bulk, and isochronous transfers for all 16 endpoints.
  - Supports USB remote wake-up feature.
  - Integrated USB transceivers for high-speed, full-speed, and low-speed operation
  - 5 V tolerant I/O buffers allow operation in 3 V or 5 V environments.
- 4K x 32 on-chip ROM for code storage.
- 2K x 32 on-chip RAM.
- On-chip PLL generates high-speed clocks from 12 MHz external source.
- External memory interface (EMI) to off-chip memory-mapped devices.
- AMBA AHB system bus and APB peripheral bus.
- I^2C interface for non-volatile configuration
- Audio interfaces:
  - 4 I^2S stereo inputs supporting rates to 24-bit, 96kHz
  - 4 I^2S stereo outputs supporting rates to 24-bit, 192kHz
  - I^2S input/output configurable for AC'97 operation
  - IEC-958 (S/PDIF) input and output supporting 32kHz, 44.1kHz, 48kHz, and 96kHz
- 16-bit timer.
- Reset/clock/power management.
- Decoder controls the selection of on-chip slave blocks.
- Arbiter allows for multi-master capability of the device.
- Programmable interrupt controller (PIC) provides capability to prioritize and mask interrupts.
- Test/debug block for software development support.
- Embedded ICE/JTAG for ARM7TDMI core testing.
- Interrupt controller (IC).
- Power control.

Goals

The USS2827 is being defined as a standard product for Agere tha can be used in several different application areas:

- A simple USB 2.0 device controller used to provide the USB interface and protocol handling for a client device where another processor is present.
- As the main processor in a USB client device. In this case, the processor in the USS2827 is used to run other system code in addition to the USB protocol stack.
- A USB 2.0 dial-up V.92 modem. The device has a simplified AC '97 interface that can be used to connect a low-cost SV92A3/CSP1035A soft modem chip set.

Two versions of the device are planned. A low-cost version in a 48-pin TQFP package without an external memory interface will handle simple device controller and modem operation using only the on-chip ROM and RAM. For applications that required additional memory or customer-developed application code, a 100-pin device with a 16-bit wide memory bus will be offerred at a premium price. The 100-pin device will also be used by Agere as a development vehicle for future ROM codes for the on-chip memory.

System Architecture

Figure 1 shows a block diagram of the USS2827 Device Controller. The device is based on an ARM7TDMS core and uses an AHB bus for the high-speed memories and peripherals. One of the design guidelines for the device is use single-clock synchronous logic. The AHB was choosen over an ASB bus for this reason. Low-speed peripherals are connected via an APB bus.

The sub-sections following the block diagram describe the various interfaces on the USS2827 and the major internal blocks of the device.

Interfaces

The following subsections describe the various interfaces on the USS2827. All interfaces except the external memory interface are present on the 48-pin version of the device.

ARM Test/Debug

This is the standard 5-wire JTAG interface used by the ARM development tools for loading and debugging software. This interface can also be used for loading production tests.

USB 2.0 Interface

The USB interface is the two wire differential interface (D-plus and D-minus) plus dedicated VDD and VSS pins.

EEPROM Interface

The EEPROM interface is a two wire I2C bus. Typically, the serial EEPROM is used to store small amounts of configuration information such as ID's, serial numbers, etc.

Crystal Interface

The USS2827 uses an inexpensive external 12 MHz crystal. This interface includes the two crystal connections (CKI, CKI2) as well as dedicated VDD and VSS pins.

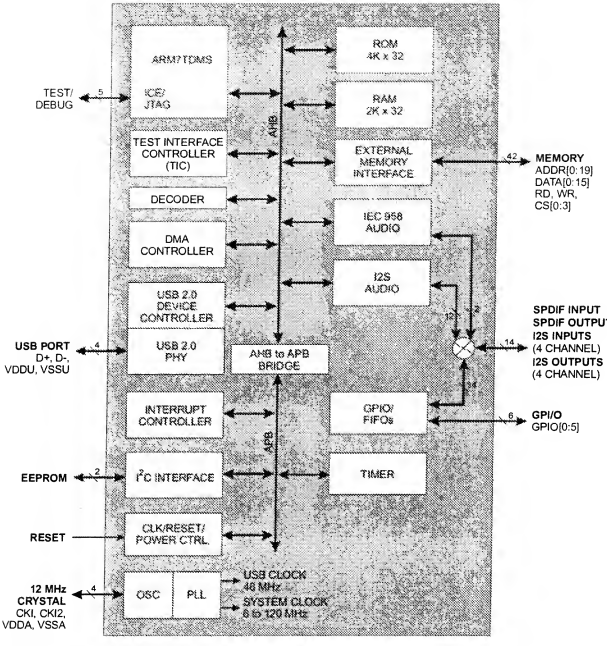

Figure 1. USS2827 Block Diagram.

General Purpose I/O and FIFO's

The GPIO and FIFO interfaces are actually two separate interfaces multiplexed together in order to reduce pin count. When the 2827 is used as a simple device controller, an external processor connects to the GPIO/FIFO interface in order to effeciently pass data over an 8-bit bus. In other applications, the port can be configured as general-purpose I/O's for connecting to external hardware.

I^2S Audio Interface

The USS2827 will support 8 channels of audio input and 8 channels of audio output on I2S interfaces (organized as 4 stereo inputs and 4 stereo outputs). The USS2827 operates as the master for all channels.

The input channels will support rates to 96 KHz and resolution to 24 bits. It is assumed that the input channels will all be configured for the same sample rate and resolution so that the SCK and WS signals can be common across the 8 input channels.

The output channels will support rates to 192 KHz and resolution to 24 bits. It is assumed that the output channels will all be configured for the same sample rate and resolution so that the SCK and WS signals can be common across the 8 output channels.

Note that this does leave the option of configuring the input and outputs at separate rates and resolutions if the application requires.

This interface can optionally be configured as two AC '97 (host) channels with the required capabilities to allow the connection of typical AC '97 audio and modem codecs. The interface should work with Agere's CSP1037D, Scorpio, SV92A2, and SV92A3 AC '97 soft modem devices (assume that the modem device is in secondary mode and the USS2827 provides the required clocks).

IEC 958 Audio Interface

The USS2827 has a single IEC 958 (aka S/PDIF) input and a single output capable of supporting 32kHz, 44.1kHz, 48kHz, and 96kHz data.

Block Definitions

The following sections describe the major blocks in the USS2827 device.

ARM7TDMS Core

The ARM7TDMS core will run at clock speeds up to 120 MHz and from the on-chip memory will yield 60 MIPs of performance. A JTAG interface is provided for connecting to the ARM development tools.

On-Chip ROM and RAM

There is 4Kx32 ROM and 2Kx32 RAM on chip accessible with zero wait states. With the 48-pin device, this is the only memory available to the ARM core.

External Memory Interface

The external memory interface is available only on the 100-pin package. This is a 16-bit wide memory bus with 20 address lines. There are four chip selects available to select external Flash ROM, RAM or other memory devices. The starting memory address and length for each device select strobe is programmable as are wait states. This allows the use of mixed on-chip and external memories.

Test Interface Controller (TIC)

A standard test interface controller is available to the ARM core to assist with production testing of the device.

Programmable Timer

A programmable timer is available to the ARM7 to enable the use of real-time OS's and for other use. The timer is programmable in increments of the 12 MHz clock period.

USB 2.0 PHY

The USB 2.0 PHY used on the USS2827 is similar to the USS2X1 standalone 2.0 phy device. The main difference is the process technology. In order to allow prototyping of the USS2827 in FPGA using an external USS2X1 phy device, the internal architecture and interface to the 2.0 Phy should mimic the USS2X1.

USB 2.0 Device Controller

The actual USB 2.0 device controller block used on the USS2827 has yet to be determined. There are several sources for standard USB 2.0 device controllers that can be used with the USS2X1 phy and it is assumed that we will re-use an available block rather than create a new one.

Programmable Interrupt Controller

The programmable interrupt controller will consolidate the various interrupt sources from within the USS2827 and allow them to be independently enabled by the ARM core.

I^2C Interface

The Inter Integration Circuit (I^2C) interface is a two-wire bi-directional serial bus that is capable of providing simple and efficient communication between devices. A single industry-standard EEPROM device will be interfaced to OCM through I^2C.

I^2C features supported in this design:

- Uses the AMBA APB protocol (ver.2.0)
- Uses I^2C bus specification (ver.2.1)
- Two data rates supported, 100Kbps and 400Kbps
- Single Master operation supporting multiple slave devices
- Programmable for normal or extended addressing (7-bit or 10-bit).
- Transfer status interrupts and flags

The I^2C interface module proposed for OCM features both an AMBA APB and an I^2C interface. The APB ports interface the I^2C module to an internal SoC APB bus. External devices that are connected to an I^2C bus can be interfaced to the module through the two bi-directional I^2C ports.

Standard I^2C features **not supported** in this design:

- High speed data rate, 3.4Mbps
- Multiple Master operation
- Bus Arbitration
- Clock Synchronization

Crystal Interface

An external 12 MHz crystal provides the clock source for the device with an internal PLL to generate the required 48 MHz clock for the USB interface. Note that the PLL is a simple "x4" block. The other rates are generated by dividing the 48 MHz clock.

Clock and Power Control

An on-chip power-up reset generator works in conjunction with an external RESET signal to control the internal reset of the device. The ARM clock for the ARM core can be selected as the 48 MHz clock or lower rates or 6, 12 or 24 MHz which are generated by enabling clock dividers.

At power-up, the crystal interface is enabled and the PLL is disabled. The ARM7 core runs at the 12 MHz crystal rate and boots from on-chip ROM.

There are independent clocks for most peripherals on the USS2827, allowing blocks not required in any specific mode to be disabled in order to minimize power dissipation.

I^2S Audio Interface

The I2S audio interface connects to the ARM AHB bus and provides 4 channels of stereo input and 4 channels of stereo output that are independently configurable. Sufficient hardware fifo's are provided for both inputs and outputs to ensure that data streams are not corrupted due to ARM software latencies.

This interface can optionally be configured as two AC '97 (host) channels with the required capabilities to allow the connection of typical AC '97 audio and modem codecs.

IEC 958 Audio Interface

The ISC 958 audio interface connects to the ARM AHB bus and provides a single input and output. Sufficient hardware fifo's are provided for both input and output to ensure that data streams are not corrupted due to ARM software latencies.

Exh. 2

AGERE SYSTEMS INVENTION SUBMISSION

This invention submission is being provided to an attorney in order to determine how to protect intellectual property and to facilitate efforts to acquire appropriate protection. Distribution of this invention submission shall be limited to attorneys and persons acting on behalf of Agere to facilitate making such determinations.

Name(s) of Submitters	Telephone No:	Loc/Room	SBU/Org. Title:	HR ID:	E-Mail Address
Daniel Devine	610-712-6802	12B-284	CCD-Wired	7499627	dandevine@agere.com

TITLE: ARM7 Processor based USB 2.0 Device Controller

Important Notes: (1) Keep in mind that your submission should be written so it can be understood in 5 to 10 minutes by a generalist. Avoid the use of undefined acronyms and jargon. Keep the language simple. (2) Have any of the above submitter(s) discussed this invention with, or provided an invention submission disclosing this invention to, an attorney other than the recipient of this invention submission? ____YES ____NO

IP LAW USE
Submission No: 124809
Date Received: July 11, 2003
Attorney: Robert P. Marley

1. Describe the problem your invention solves:

An ARM7 Processor based USB 2.0 device controller provides a flexible platform for computer peripheral manufacturers to quickly and cost-effectively implement USB 2.0 PC interconnect technology into their products.

2. Based on information of which you are already aware, describe:

(i) previous attempts to solve the problem your invention solves:

previous attempts with on-board processors proved to be under-powered. With an ARM7 processor on-board, it is now possible to eliminate the current processor in the PC peripheral.

(ii) the disadvantages of the previous attempts:

Lack of MIPs (millions of instructions per second) in previous attempts meant that the USB 2.0 device could only provide the USB 2.0 functionality, but not the functionality of the peripheral, be it a camera, scanner, printer, etc.

3. Summarize (30 words or less) the new feature(s) of your invention that solve the problem:

By integrating a powerful ARM7 processor this invention solves the problem by off-loading the existing peripheral processor to the point that processor can be eliminated from the architecture resulting in less cost and smaller form factor.

4. Succinctly describe your invention, referring to drawings, sketches, photographs, etc., in sufficient detail to enable one knowledgeable in the invention's field of technology to understand construction and operation of the invention. Drawings, etc., should show only those features necessary for an understanding of the invention. Describe how/why your invention overcomes the disadvantages noted in 2. (ii) above.

The USS2828 USB 2.0 Device controller is a product targeted at the rapidly growing market for USB 2.0 Peripherals. It is estimated the silicon market size is $487M, of which Agere could capture 13% share, or at least $61M over a 3 year period.

The USS2828 shall:

- Provide customers a complete, certified USB 2.0 peripheral solution including software and a powerful microprocessor.
- Be a lead for USB 2.0 device IP development for Agere Integrated ASICs for:
  - Oak Technology ASIC
  - Hermes 3 (802.11 MAC)
  - Two-Wire ASIC

- The processor in the USS2828 shall provide additional MIPs over and above that required for fundamental USB 2.0 traffic processing.
- The additional MIPs shall provide customers with the opportunity to remove their existing peripheral microprocessor, thereby eliminating cost and form factor.
- The USS2828 will be used as a USB 2.0 soft modem device with the potential to sell 1 million units per year.
- Competitive advantage shall be provided by Agere's superior software algorithm capabilities which will allow for higher (value) pricing.

The USS2828 shall be manufactured in the lowest available cost technology including up-front mask costs, recurring costs, and risk (as it relates to TTM - Time to Market)

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USS2827 Block Diagram

5. Advantages of your invent

Improved Cost and form factor (size) can be achieved via the use of this type of device. The integration of a powerful ARM7 processor off-loads the existing peripheral processor to the point that the existing peripheral processor can be eliminated from the architecture.

6. Explain how use of your invention would be detected:

A de-capping of a USB 2 peripheral device would show an ARM7 block on the die, along with circuitry to a USB 2.0 connection.

Submitter(s) signature(s) and date:

_____ _____
date

_____ _____
date

_____ _____

This invention submission has been read and understood by the following two witnesses:

_____ _____
date

_____ _____
date

ATTORNEY-CLIENT PRIVILEGED DOCUMENT

*** Provide the information requested in this box on each page of the submission, as well as drawings, sketches, photographs, etc ***

Exh. 3

Kevin Mason

From: Devine, Daniel J (Dan) [dandevine@agere.com]
Sent: Monday, January 12, 2004 2:22 PM
To: kmm@rml-law.com
Subject: MRD & SRD

Hi Kevin;

Nice meeting you today. As requested please find the SRD and MRD for the USS2827 device.

Please let me know if there is anything else you might need.

Thanks;

Dan

<<USS2827___2828_StdProductMRDAug2003Rev_0[1].95.doc>> <<USS2828_SRD_12162003.doc>>

Exh. 4

Kevin Mason

From: Devine, Daniel J (Dan) [dandevine@agere.com]
Sent: Tuesday, February 03, 2004 3:43 PM
To: kmm@rml-law.com
Subject: Patent Form & Block Diagram

<<USB2devicepatentform.doc>> <<USS2828PatentSlides.ppt>>

Hi Kevin;

Please let me know what else you need. Just an FYI, we were in the process of created two versions, one for a customer with lots of audio capability (the USS2827) and one for use in simpler peripherals and as a USB 2 soft modem (the USS2828).

Thanks;
Dan

Exh. 5

Subject: RE: Agere Patent Matter 124809
From: "Devine, Daniel J (Dan)" <dandevine@agere.com>
Date: Mon, 23 Feb 2004 09:33:29 -0500
To: "Kevin M. Mason" <kmm@rml-law.com>

Hi Kevin;

I thought I had responded to you via email on this.

The draft is fine, go with it.

Thanks;
Dan

-----Original Message-----
From: Kevin M. Mason [mailto:kmm@rml-law.com]
Sent: Monday, February 23, 2004 8:02 AM
To: Devine, Daniel J (Dan)
Subject: Re: Agere Patent Matter 124809

Hi Dan:
How is your review coming along on the patent draft? We'd really like to get the application filed this week (which means we need to get the application to the Managing Attorney for review as soon as possible).
Regards, Kevin

Kevin M. Mason wrote:

> Hi Dan:
> I attach a draft of the above application for your review. Please carefully review the enclosed application to ensure that it is clear and complete, sets forth the best mode contemplated by each inventor for carrying out the invention, and contains a sufficient disclosure to enable a person of ordinary skill in the art to make and use the invention. There is some additional work to be done on my end. If possible, I'd like to discuss your comments early next week, so that I
>
> can turn around another (hopefully, final) draft before I leave for vacation on 2/12.
>
> Please let me know if you have any questions or comments. Best regards, Kevin

Exh 6

Subject: RE: Devine 2
From: "Devine, Daniel J (Dan)" <dandevine@agere.com>
Date: Mon, 23 Feb 2004 21:42:33 -0500
To: "Kevin M. Mason" <kmm@rml-law.com>

Kevin;

Thanks for your efforts on this.

It looks good.

Dan

-----Original Message-----
From: Kevin M. Mason [mailto:kmm@rml-law.com]
Sent: Monday, February 23, 2004 5:38 PM
To: Devine, Daniel J (Dan); Marley, Robert P (Bob)
Subject: Devine 2

Genetlemen:
I attach a final draft of the above application for your review. Please carefully review the enclosed application to ensure that it is clear and complete, sets forth the best mode contemplated by each inventor for carrying out the invention, and contains a sufficient disclosure to enable a person of ordinary skill in the art to make and use the invention. We'd like to file this application by Friday, Feb. 27, 2004.

Please let me know if you have any questions or comments.
Best regards,
Kevin